REMARKS

The Examiner has provisionally rejected Claims 1, 13-15, 19-21, 51-52 under 35 U.S.C. 101 as claiming the same invention as that of Claims 1-34 of co-pending Application No. 09/885,382. Submitted herewith is a terminal disclaimer for obviating this provisional rejection.

The Examiner has further rejected Claim 11 under 35 U.S.C. 112, second paragraph, as being indefinite in the use of the term "swizzle", and failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response, applicant has clarified the claims to avoid this rejection. Support for such amendment may be found on Page 19 of the originally filed specification

The Examiner has rejected Claims 1-13, 15-22, 26, 30-34, 37, 51-52 under 35 U.S.C. 102(b) as being anticipated by Read, U.S. Patent 5,689,695. Applicant respectfully disagrees with such rejection.

In particular, the Examiner relies on the following excerpt from Read to show applicant's claimed "swizzle operation."

> "This combined register A14/A6 will generally be used as a stack pointer. Note that stack operations are only allowed on aligned 32 bit word boundaries. Consequently the two least significant bits of combined register A14/A6 are hardwired to "00". Writing to these two bits has no effect and they are always read as "00". Registers A7 and A15 are also embodied by the same hardware and both global address sun-unit 610 and local address unit 620 may use this combined register in the same instruction. Register A7 is accessible to local address unit 620 and register A15 is accessible to global address unit 610. Combined register A15/A7 is hardwired to all "0's"."
> (col. 81, lines 33-46)

This excerpt, however, simply fails to disclose, teach or suggest any sort of "swizzle operation," let alone a "swizzle operation utilizing component re-mapping." Only applicant teaches and claims such a swizzle operation in the context of a programmable instruction set with "branching" and/or "condition codes."

It further appears that the Examiner has not specifically addressed Claim 21. However, the Examiner does address Claim 12 by attempting to show a couple of the following claimed operations in the prior art.

> "a branch operation, a call operation, a return operation, a cosine operation, a sine operation, a floor operation, a fraction operation, a set-on-equal-to operation, a set false operation, a set-on-greater-than, a set-on-less-than-or-equal operation, a set-on-not-equal-to operation, a set true operation, a no operation, address register load, move, multiply, addition, multiply and addition, reciprocal, reciprocal square root, three component dot product, four component dot product, distance vector, minimum, maximum, set on less than, set on greater or equal than, exponential base two (2), logarithm base two (2), exponential, logarithm, and/or light coefficients" (see Claim 21)

The Examiner has not, however, shown in the prior art a combination of at least ten (10) of such operations in the context of a "computer graphics pipeline" for "performing [the] programmable operations on the data in order to generate output, wherein the operations are programmable by a user utilizing instructions from a predetermined instruction set."

Applicant emphasizes that such a specific set of at least ten (10) of such specific operations provides an enhanced "computer graphics pipeline" that is capable of accomplishing advanced tasks not envisioned at the time of Read, in a programmable manner. Simply nowhere in the prior art is there such a combination of features for fulfilling the foregoing objectives. A specific showing of such combination of operations or a notice of allowance is respectfully requested.

Still yet, it appears that the Examiner has not addressed the subject matter of Claims 34, and 51-52. In particular, in none of the references relied upon by the Examiner is there any sort of method for executing a function including "pre-processing the input data based on the function to be executed on the input data," "processing the input data utilizing a plurality of operations independent of the function to be executed on the input data," and "post-processing the input data to generate output data." (emphasis added). Simply nowhere in the prior art is there

taught, disclosed or suggested such a specific 3-part method for executing a function.

The Examiner has further rejected Claims 23-25, 27-29, 35-36, 38-50 and 53 under 35 U.S.C. 103(a) as being unpatentable over Read, U.S. Patent 5,689,695, and further in view of Choe, et al., U.S. Patent 6,385,632. Applicant respectfully disagrees with such rejection, especially in view of the amendments made hereinabove.

In particular, applicant has amended independent Claims 22, 31-33 to include the subject matter of Claim 25. It appears that the Examiner has failed to address applicant's claimed "mathematical function [that] is a function in which an initial *n* derivatives are capable of being tabulated and accessed via an interpolation operation," as such limitations are not discussed in the Examiner's action and Choe, as well as the remaining references, simply fails to disclose, teach or suggest the same. Simply nowhere in the prior art is there such a combination of features for providing an improved calculation technique.

Still yet, it appears that the Examiner has not addressed the subject matter of Claims 53 with any sort of specificity. For example, in none of the references relied upon by the Examiner is there any sort of method for executing a function including "identifying a sign, an exponent, and a mantissa associated with the input data utilizing the computer graphics pipeline," "normalizing the input data utilizing the computer graphics pipeline," "if the function includes an exponent function, executing a barrel shift operation on the input data utilizing the computer graphics pipeline," "if the function includes a cosine function, adding a one (1) to the phase of the input data utilizing the computer graphics pipeline," "if the function includes at least one of a sine function and a cosine function, multiplying the input data by (1/(2p) + 1) and performing a conditional 1's complement operation on the input data utilizing the computer graphics pipeline," "extracting a set of most significant bits and a set of least significant bits from the mantissa associated with the input data utilizing the computer graphics pipeline," "adding a one (1) to the most significant bits utilizing the computer graphics pipeline," "looking up a plurality of derivatives based on the most significant bits utilizing the computer graphics pipeline,"

"calculating a Taylor Series with the derivatives and the least significant bits utilizing the computer graphics pipeline," "post-processing the input data to generate output data utilizing the computer graphics pipeline," etc.

An allowance or a specific showing in the prior art of applicant's claimed invention is therefore respectfully requested.

For payment of the fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP055/P000369).

Respectfully submitted,

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